In the Claims:

1. (Currently Amended) An apparatus, comprising:

an array of tag address storage locations; and

a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache ~~associated with~~ located on a memory module, the command sequencer and serializer unit to reduce a first plurality of address and command signals down to a more narrow set of signal lines coupled to the memory module, the more narrow set of signal lines forming a point-to-point interconnect between the command sequencer and serializer unit and the memory module, the command sequencer and serializer unit to cause a current line of data to be read out of a memory module memory device and to load a next line of data from the memory module memory device to the data cache.

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2. Cancelled

3. (Currently Amended) The apparatus of claim ~~2~~ 3, the command sequencer and serializer to deliver a read and preload command to the data cache ~~associated with~~ located on the memory module, the read and preload command to cause the current line of data to be read out of the memory module memory device and to load the next line of data from the memory module memory device to the data cache.

4. (Original) The apparatus of claim 3, the read and preload command including memory module destination information, way information, address strobe state information, and cache hit information.

5. (Original) The apparatus of claim 4, the read and preload command further including column address information and memory device bank information.

6. (Original) The apparatus of claim 5, the read and preload command information delivered over four transfer periods.

7. (Original) The apparatus of claim 6, the cache hit information and way information transferred during the fourth transfer period.

8. (Currently Amended) ~~An apparatus~~ A memory module, comprising:

at least one memory device; and

a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by a memory controller component over a memory bus, the memory controller component including an array of tag address storage locations, the plurality of commands including a read and preload command to cause a current line of data to be read out of the memory device and to load a next line of data from the memory device to the data cache.

9. Cancelled

10. Cancelled

11. (Currently Amended) The ~~apparatus of claim 10~~ memory module of claim 8, the read and preload command including memory module destination information, way information, address strobe state information, and cache hit information.

12. (Currently Amended) The ~~apparatus~~ memory module of claim 11, the read and preload command further including column address information and memory device bank information.

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13. (Currently Amended) The ~~apparatus~~ memory module of claim 12, the read and preload command information received over four transfer periods.

14. (Currently Amended) The ~~apparatus~~ memory module of claim 13, the cache hit information and way information transferred during the fourth transfer period.

15. (Currently Amended) A system, comprising:

a processor;

a memory controller coupled to the processor, the memory controller including

an array of tag address storage locations, and

a command sequencer and serializer unit coupled to the array of tag address storage locations; and

a memory module coupled to the memory controller via a memory bus, the memory module including

at least one memory device, and

a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, one of the plurality of commands including a read and preload command to cause a current line of data to be read out of the memory device and to load a next line of data from the memory device to the data cache.

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16. (Original) The system of claim 15, the memory module further including a command decoder and deserializer unit to receive command and address information from the memory controller, the command decoder and deserializer unit providing control for the data cache.

17. Cancelled

18. (Currently Amended) The system of claim ~~17~~ 16, the read and preload command including memory module destination information, way information, address strobe state information, and cache hit information.

19. (Original) The system of claim 18, the read and preload command further including column address information and memory device bank information.

20. (Original) The system of claim 19, the read and preload command information delivered over four transfer periods.

21. (Original) The system of claim 20, the cache hit information and way information delivered during the fourth transfer period.

22. (Original) The system of claim 15, a point-to-point interconnect to couple the memory controller to the memory module.

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23. Cancelled

24. Cancelled

25. Cancelled

26. Cancelled

27. Cancelled